Analysis and Design of MOSFET based Amplifier in Common Source Configurations

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This paper presents the design of amplifier in Common Source configuration. It also presents its input and output characteristics, time domain analysis and frequency response of the amplifier. The voltage gain of amplifier is designed by choosing appropriate value of V_{GS} in saturation region in the input output voltage characteristics. After choosing that value we applied an input sinusoidal signal and check the output waveform and compare it with the theoretical results.

Keywords: CMOS Analog Integrated Circuits, T-Spice, Voltage Swing, Overdrive.

1. INTRODUCTION

Amplification is an essential function in most analog (and many digital) circuits. We amplify an analog or digital signal because it may be too small to drive a load, overcome the noise of a subsequent stage, or provide logical levels to a digital circuit. Amplification also plays a critical role in feedback systems. In this paper, we study the low-frequency behavior of single-stage CMOS amplifiers. Analyzing both large signal and small signal characteristics of circuit, we develop intuitive techniques and models that prove useful in understanding more complex systems. An important part of designer's job is to use proper approximations so as to create a simple metal picture of a complicated circuit.

2. COMMON SOURCE AMPLIFIER

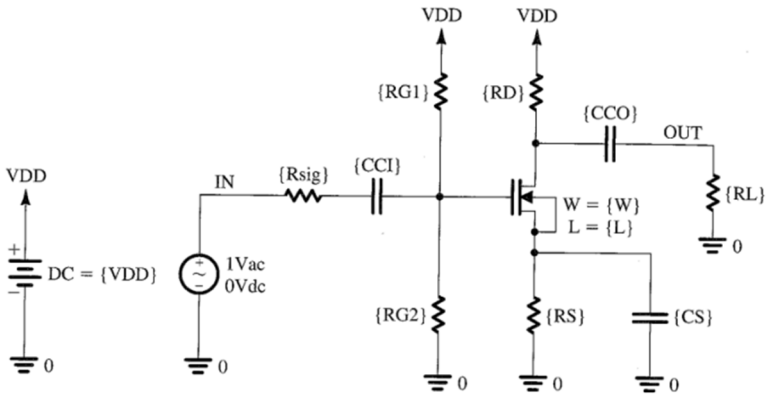

Fig. 1: Schematic of CS Amplifier.

The Common-source (CS) configuration is the most widely used of all MOSFET amplifier circuits. Observe that to establish a signal ground we have connected a large capacitor, C_S, between the source and ground. This capacitor, usually in uF range, is required to provide very small impedance at signal frequencies of interest. In this way, the signal current passes through C_S to ground and thus bypasses the resistance R_S, Hence C_S is called bypass capacitor. A common source amplifier realized using the circuit of Figure 1.

In order not to disturb dc bias current and voltages, the signal to be amplified, shown as voltage source V_{sig} with an internal resistance R_{sig}, is connected to the gate through a large capacitor C_{C1}. Similarly, the drain is also connected to load resistance R_L via a large capacitor C_{C2}. These two capacitances are called coupling capacitors. Note that R_L can either be a load resistor, to which the amplifier is required to provide its output voltage signal, or it can be the input impedance of another amplifying stage. The resistances R_{G1} and R_{G2} are used to provide a suitable dc bias to the transistor to make it operate in saturation region.

In this paper we will use TSpice tool to compute the voltage gain and frequency response of the CS amplifier. Here we connected source and body of the MOSFET together to cancel the body effect. Also, we used the 2-um CMOS technology and Spice level-1 parameters.

The expressions for voltage gain(A_V) and Input Impedance R_{in} of CS amplifier is given by

$$A_V = -g_m(r_{ds} \| R_D \| R_L) \tag{1}$$

$$R_{in} = R_{G1} \| R_{G2} \tag{2}$$

Firstly, we will draw voltage transfer characteristics (VTC) of the amplifier. We will observe the change output voltage with respect to the change in input voltage. This will gives us the insight of choosing appropriate value of V_{GS} (operating point) so that our transistor works in saturation region and gives us maximum voltage swing.

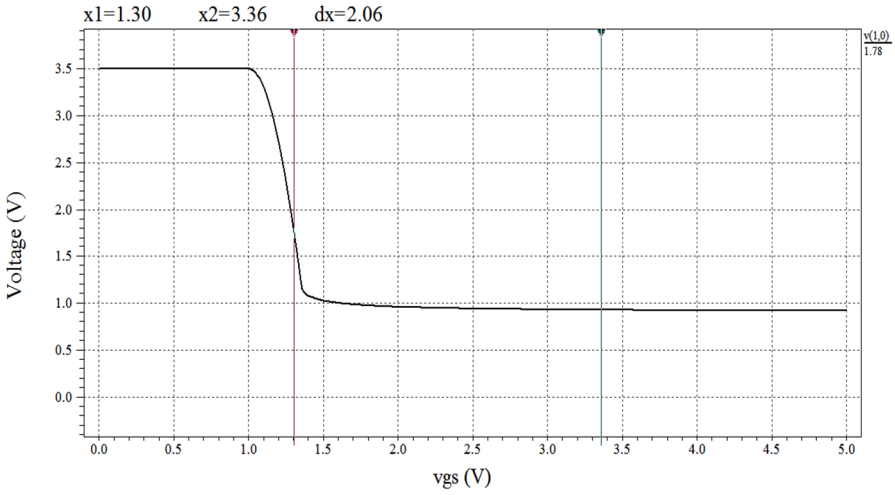

Fig. 2: Voltage Transfer Characteristics (VTC)[A] of CS Amplifier.

Now, we will choose V_{GS} as such that our transistor works in saturation region. Here saturation region of the transistor lies between 1V to 1.4V. So, we choose V_{GS}= 1.3V to ensure that our transistor works in saturation region and acts as an amplifier.

We applied an input signal of 1mV and frequency 1 KHz. Our target is to amplify this signal 10 times; i.e Amplifier Gain should be 10. We assume that power supply V_{DD}=3.5V and maximum power consumption P=1.5mW. We will also assume a signal source resistance R_{sig} =10kΩ, a load resistance of R_L=50kΩ and bypass and coupling capacitors of 10 uF. With a 3.5V power supply, drain current of MOSFET is limited to

$$I_D = \frac{P}{V_{DD}} = \frac{1.5mW}{3.5\,V} = 4.2mA \tag{3}$$

The equation of I_D in saturation is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{ov})^2(1+\lambda V_{DS}) \tag{4}$$

$\mu_n C_{ox} = 3 \times 10^{-5}$(Spice Level-1 Parameter)

Overdrive, V_{ov}= 0.3V (Typical Value)

λ=0.02(Spice Level-1 Parameter)

$V_{DS} = \frac{V_{DD}}{3}$(For maximum Voltage Swing)

$V_{DS} = 1.16\,V$

By solving equation (4) for $\frac{W}{L_{eff}}$

$$\frac{W}{L_{eff}} = \frac{2I_D}{\mu_n C_{ox} V_{ov}^2(1+\lambda V_{DS})} \tag{5}$$

After putting all the values in eq. (5) we get

$$\frac{W}{L_{eff}} = 305 \tag{6}$$

Here, L=2 μm as per 2-μm CMOS technology node.

$$L_{eff} = L - 2L_D = 0.4\mu m \qquad \text{where } L_D = 0.8 \tag{7}$$

Therefore,

$$W = 305 \times L_{eff} = 305 \times 0.4\mu m = 122\mu m \tag{8}$$

Now, we will find drain to source resistance r_{ds}, which is given by

$$r_{ds} = \frac{1}{\lambda I_D} = 119.04\ K\Omega \tag{9}$$

The transconductance g_m of the amplifier is given by

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = 2.7\ mS \tag{10}$$

By using equation (1) we will find the value of R_D, as A_V=10 is given

$$A_V = -g_m(r_{ds} \| R_D \| R_L) \tag{11}$$

Using all the values given, R_D calculated as

$$R_D = 4.13\ K\Omega \tag{12}$$

Output voltage V_O is given by

$$V_O = V_{DD} - I_D R_D = 3.5 - (0.42 \times 1.43) = 1.76\ V \tag{13}$$

Source Resistance R_S can be written as

$$R_S = \frac{V_O - \frac{V_{DD}}{3}}{I_D} = 1.42\ K\Omega \tag{14}$$

For finding Gate voltage V_G we apply KVL at the input loop which gives

$$V_G = I_D R_S + V_{OV} + V_{th} = 1.89\ V \tag{15}$$

We use hit and trail method for finding R_{G1} and R_{G2} so it can satisfies this equation

$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD} \tag{16}$$

This gives,

$$R_{G1} = 2\ M\Omega \tag{17}$$

$$R_{G2} = 2.35\ M\Omega \tag{18}$$

With the help of above results we design CS amplifier on TSpice tool. After doing its transient analysis we get the output signal waveform with respect to input signal. Also the input signal is amplified 10 times as shown in Figure 3.

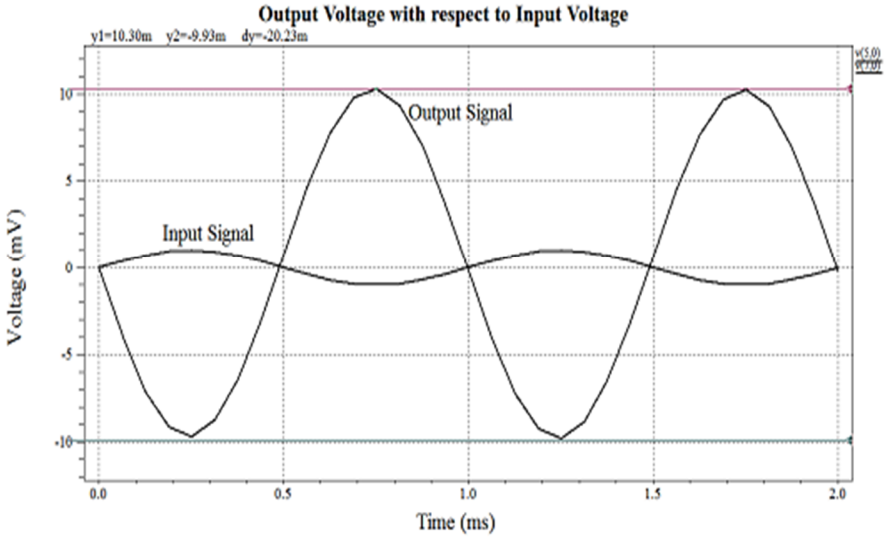

Fig. 3: Output Voltage with respect to Input Voltage[B].

We have applied the input signal of 2mV P-P and get the output voltage of 20.23mV. i. e

$$V_{in} = 2\,mV \quad (P-P) \tag{19}$$

$$V_O = 20.23\,mV \quad (P-P) \tag{20}$$

Therefore, Voltage Gain A_V is

$$A_V = 10.11 \quad (Practical) \tag{21}$$

We get our practical gain of 10.11 as our theoretical gain is 10. Therefore, % error is given by

$$\%error = \frac{A_V(Th.) - A_V(Pr.)}{A_V(Th.)} \times 100 \tag{22}$$

$$\%error = \frac{10 - 10.11}{10} \times 100 = -1.1 \tag{23}$$

Next, to measure the mid-band gain A_M and the 3-dB frequencies f_L and f_H, we apply a 1-V ac voltage at the input, perform an ac analysis simulation, and plot the output voltage magnitude versus frequency as shown in Figure 4.

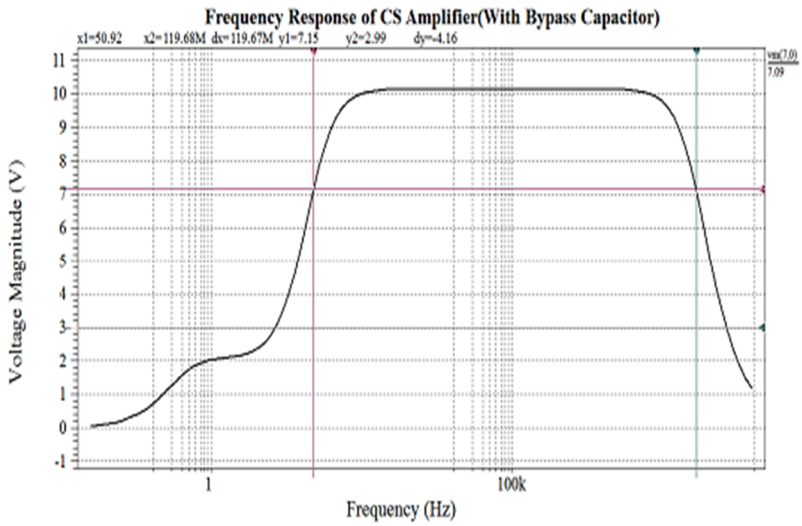

Fig. 4: Frequency response of CS amplifier with Bypass capacitor[C].

This corresponds to the magnitude response of CS amplifier because we chose a 1-V input signal. Accordingly, the mid-band gain A_M=10.11 and the 3-dB frequencies are f_L=50.92Hz and f_H=119.68MHz. Therefore, bandwidth (BW) is

$$B_W = f_H - f_L \approx 119.68\,MHz \approx 120\,MHz \tag{24}$$

The effect of bypass capacitor C_S is seen clearly from the graph. Because gain is flattens at very low frequency, i.e 10Hz. This flattening of gain is due to capacitor C_S and resistor R_S. Now, we will see the effect of unbypassed resistor R_S, i.eC_S=0. This will reduce the gain of the amplifier by a factor of $1+g_mR_S$ and increase the bandwidth (BW) of the amplifier. The effective reduction of gain and increment of bandwidth (BW) is shown in Figure 5.

$$A_{V1} = -g_m \frac{(r_{ds} \| R_D \| R_L)}{1+g_m R_S} \tag{25}$$

$$1 + g_m R_S = 4.834 \tag{26}$$

$$A_{V1} = -g_m \frac{(r_{ds} \| R_D \| R_L)}{4.834} \tag{27}$$

A_{V1}→ Gain without bypass capacitor C_S.

The mid-band gain in this case is A_M=2.09 and the 3-dB frequencies are f_L=0.29Hz and f_H=415.86MHz. Therefore, bandwidth (BW) is

$$B_W = f_H - f_L \approx 415.86\,MHz \approx 416\,MHz \tag{28}$$

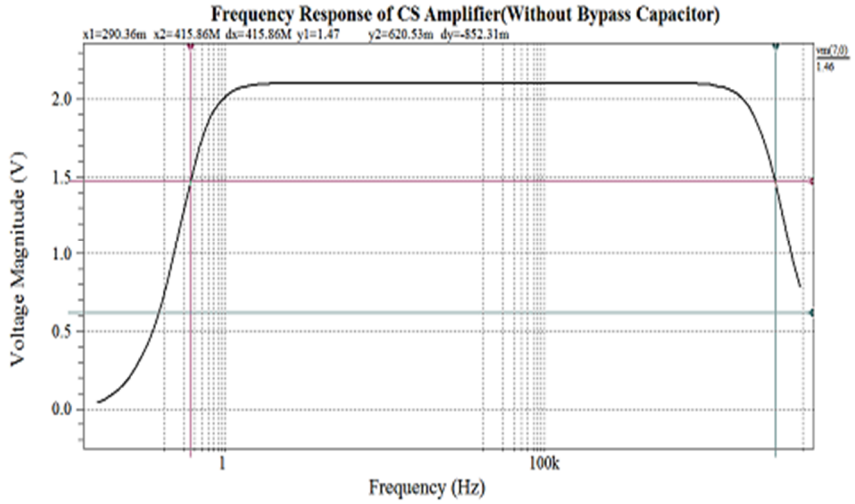

Fig. 5: Frequency response of CS amplifier without Bypass capacitor[D].

So, we can see clearly that the bandwidth is increased by three fold and gain is reduced by a factor of 4.8. Therefore, the source degeneration resistor R_S provides negative feedback, which allows us to trade off gain for wider bandwidth.

3. CONCLUSION

In this paper, we accomplished the goal of learning and designing of the different types of amplifiers. i.e common source, common drain, common gate using T-Spice tool. We have seen their frequency response to check in which frequency range our amplifier gives the optimal gain. We also seen the effect of different biasing and feedback resistors on gain and drawn their plots.

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