Analysis and Design of MOSFET based Amplifer in Common Drain Configurations

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This paper presents the design of amplifier in Common Drain configuration. It also presents its input and output characteristics, time domain analysis and frequency response of the amplifier. The voltage gain of amplifier is designed by choosing appropriate value of V_{GS} in saturation region in the input output voltage characteristics. After choosing that value we applied an input sinusoidal signal and check the output waveform and compare it with the theoretical results.

Keywords: CMOS Analog Integrated Circuits, T-Spice, Voltage Swing, Overdrive.

1. INTRODUCTION

Amplification is an essential function in most analog (and many digital) circuits. We amplify an analog or digital signal because it may be too small to drive a load, overcome the noise of a subsequent stage, or provide logical levels to a digital circuit. Amplification also plays a critical role in feedback systems. In this paper, we study the low-frequency behavior of single-stage CMOS amplifiers. Analyzing both large signal and small signal characteristics of circuit, we develop intuitive techniques and models that prove useful in understanding more complex systems. An important part of designer's job is to use proper approximations so as to create a simple metal picture of a complicated circuit.

2. COMMON DRAIN AMPLIFIER

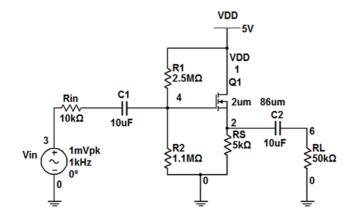


Fig. 1: Schematic of CD Amplifier.

A common drain amplifier, also known as a source follower, is one of three basic singlestage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer. In this circuit the gate terminal of the transistor serves as the input, the source is the output, and the drain is common to both (input and output), hence its name. In addition, this circuit is used to transform impedances. For example, the Thevenin resistance of a combination of a voltage follower driven by a voltage source with high Thevenin resistance is reduced to only the output resistance of the voltage follower, a small resistance. That resistance reduction makes the combination a more ideal voltage source. Conversely, a voltage follower inserted between a driving stage and a high load (i.e. a low resistance) presents an infinite resistance (low load) to the driving stage, an advantage in coupling a voltage signal to a large load. A common drain amplifier realized using the circuit of Figure 1.

In order not to disturb dc bias current and voltages, the signal to be amplified, shown as voltage source V_{sig} with an internal resistance R_{sig}, is connected to the gate through a large capacitor C₁. Similarly, the source is also connected to load resistance R_L via a large capacitor C₂. These two capacitances are called coupling capacitors. Note that R_L can either be a load resistor, to which the amplifier is required to provide its output voltage signal, or it can be the input impedance of another amplifying stage. The resistances R₁ and R₂ are used to provide a suitable dc bias to the transistor to make it operate in saturation region.

In this paper we will use TSpice tool to compute the voltage gain and frequency response of the CS amplifier. Here we connected source and body of the MOSFET together to cancel the body effect. Also, we used the 2-um CMOS technology and Spice level-1 parameters.

The expressions for voltage gain(A_V) and Input Impedance R_{in} of CD amplifier is given by

$$A_V = -\frac{g_m(r_{ds} ||R_L||R_S)}{1 + g_m(r_{ds} ||R_L||R_S)}$$
(1)

$$R_{in} = R_1 || R_2 \tag{2}$$

Firstly, we will draw voltage transfer characteristics (VTC) of the amplifier. We will observe the change output voltage with respect to the change in input voltage. This will gives us the insight of choosing appropriate value of V_{GS} (operating point) so that our transistor works in saturation region and gives us maximum voltage swing.

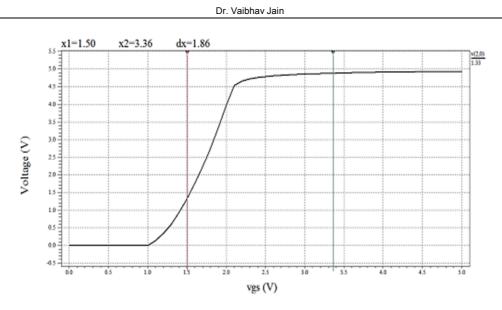


Fig. 2: Voltage Transfer Characteristics(VTC)^E of CD Amplifier.

Now, we will choose $V_{\rm GS}$ as such that our transistor works in saturation region. Here saturation region of the transistor lies between 1V to 2.9V. So, we choose $V_{\rm GS}$ = 1.5V to ensure that our transistor works in saturation region and acts as an amplifier.

We applied an input signal of 1mV and frequency 1 KHz. This is a CD amplifier or Source follower, i.e Amplifier Gain should be approximately 1. We assume that power supply V_{DD}=3.5V and maximum power consumption P=1.5mW. We will also assume a signal source resistance R_{sig}=10k Ω , a load resistance of R_L=50k Ω and bypass and coupling capacitors of 10 uF. With a 3.5V power supply, drain current of MOSFET is limited to

$$I_D = \frac{P}{V_{DD}} = \frac{1.5mW}{3.5V} = 4.2mA$$
(3)

The equation of I_D in saturation is given by

$$I_{D} = \frac{1}{2} \mu_{n} C_{ox} \frac{W}{L} (V_{ov})^{2} (1 + \lambda V_{DS})$$
(4)

 $\mu_n C_{ox} = 3 \times 10^{-5}$ (Spice Level-1 Parameter)

Overdrive, $V_{ov} = 0.3V$ (Typical Value)

λ= 0.02 (Spice Level-1 Parameter)

$$V_{DS} = \frac{V_{DD}}{3}$$
 (For maximum Voltage Swing)

 $V_{DS} = 1.16 V$

By solving equation (4) for $\frac{W}{L_{eff}}$

$$\frac{W}{L_{eff}} = \frac{2I_D}{\mu_n C_{ox} V_{ov}^2 (1 + \lambda V_{DS})}$$
(5)

After putting all the values in eq. (5) we get

$$\frac{W}{L_{eff}} = 305 \tag{6}$$

Here, L=2 µm as per 2-µm CMOS technology node.

$$L_{eff} = L - 2L_D = 0.4 \mu m$$
 where $L_D = 0.8$ (7)

Therefore,

$$W = 305 \times L_{eff} = 305 \times 0.4 \mu m = 122 \mu m \tag{8}$$

Now, we will find drain to source resistance $r_{\mbox{\tiny ds}},$ which is given by

$$r_{ds} = \frac{1}{\lambda I_D} = 119.04 \, K\Omega \tag{9}$$

The transconductance g_m of the amplifier is given by

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = 2.7 \ mS \tag{10}$$

By using equation (1) we will find the value of R_S , as $A_V=1$

$$A_V = -\frac{g_m(r_{ds} \|R_L\|R_S)}{1 + g_m(r_{ds} \|R_L\|R_S)}$$
(11)

Using all the values given, R_{S} calculated as

$$R_s = 5 K\Omega \tag{12}$$

For finding Gate voltage V_G we apply KVL at the input loop which gives

$$V_G = I_D R_S + V_{OV} + V_{th} = 2.8 V$$
(13)

We use hit and trail method for finding R_{G1} and R_{G2} so it can satisfies this equation

$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD}$$
(14)

This gives,

$$\frac{R_{G1} = 2 M\Omega}{\text{ISSN: 2249-9970 (Online), 2231-4202 (Print)}}$$

$$[69] \qquad \qquad \text{Vol. 5(1), Jan 2015}$$

Dr. Vaibhav Jain $R_{G2} = 2.6 M\Omega$ (16)

With the help of above results we design CD amplifier on TSpice tool. After doing its transient analysis we get the output signal waveform with respect to input signal as shown in Figure 3.

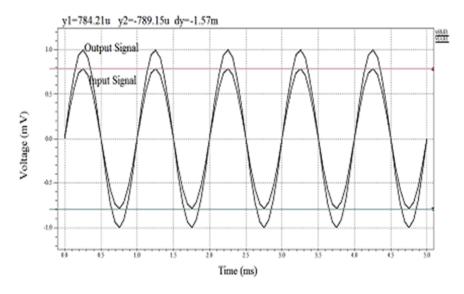


Fig. 3: Output Voltage with respect to Input Voltage^F

We have applied the input signal of 2mV P-P and get the output voltage of 1.57mV. i. e

$$V_{in} = 2 mV \quad (P - P) \tag{17}$$

$$V_0 = 1.57 \, mV \quad (P - P)$$
 (18)

Therefore, Voltage Gain A_V is

$$A_V = 0.785 \quad (Practical) \tag{19}$$

We get our practical gain of 0.785 as our theoretical gain is 1. Therefore, % error is given by

$$\% error = \frac{A_V(Th.) - A_V(Pr.)}{A_V(Th.)} \times 100$$
(20)

$$\% error = \frac{1 - 0.785}{1} \times 100 = -21.5$$
(21)

Next, to measure the mid-band gain A_M and the 3-dB frequencies f_L and f_H , we apply a 1-V ac voltage at the input, perform an ac analysis simulation, and plot the output voltage magnitude versus frequency as shown in Figure 4.

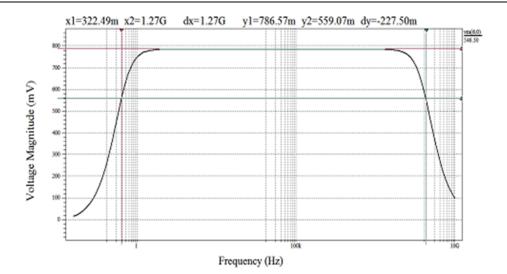


Fig. 4: Frequency response of CD amplifier^G.

This corresponds to the magnitude response of CD amplifier because we chose a 1-V input signal. Accordingly, the mid-band gain A_M =0.78 and the 3-dB frequencies are f_L= 0.32Hz and f_H=1.27GHz. Therefore, bandwidth (BW) is

$$B_W = f_H - f_L \approx 1.27 \, MHz \tag{22}$$

3. CONCLUSION

In this paper, we accomplished the goal of learning and designing of the different types of amplifiers. i.e common source, common drain, common gate using T-Spice tool. We have seen their frequency response to check in which frequency range our amplifier gives the optimal gain. We also seen the effect of different biasing and feedback resistors on gain and drawn their plots.

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Vol. 5(1), Jan 2015