

## The Study of Channel Thermal noise in MOSFETs

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*In the present paper we studied experimentally the channel thermal noise in MOSFETs of short and long channel length at various drain to source voltage ( $V_{ds}$ ) and various gate to source voltage ( $V_{gs}$ ). We also plot graph between channel thermal noise ( $S_{ID}$ ) Vs ( $V_{ds}$ ) & channel thermal noise ( $S_{ID}$ ) Vs gate to source voltage ( $V_{gs}$ ). The result so obtained has good agreement with the theoretical data available in the literature. This proves the validity of our MOSFETs model.*

**Keywords:** Channel thermal noise, MOSFETs model.

### 1. INTRODUCTION

Noise can be defined in an electrical sense as any unwanted form of energy tending to interfere with proper and easy reception and reproduction of wanted signals. Many disturbances of an electrical nature produce noise in receivers, thereby modifying the signal in an unwanted manner.

There are various ways of classifying noise. It may be subdivided according to the type, source, effect or relation to the receiver, depending on the circumstances. It can be broadly classified into two categories. They are a) external noise and b) internal noise [1,2].

**a) External noise:** It is the noise whose sources are external to the receiver. The various forms of noise created outside the receiver come under the heading external noise and include atmospheric, extraterrestrial and industrial noise.

**a.1. Atmospheric noise** – It consists radio waves which induce voltages into the antenna. The majority of these radio waves come from natural sources of disturbance, they represent atmospheric noise, generally called static. Static is due to lightning discharges in thunderstorm and other natural electric disturbances occurring in the atmosphere.

**a.2. Extraterrestrial noise** – There are almost as many types of space noise as sources. But, it can broadly be divided into two groups.

**a.2.1. Solar noise** – The sun throws so many things our way that we should not be surprised to find that the noise is noticeable amongst them. It is of two types. Under normal or quiet conditions, there is a constant noise radiation from the sun because it is a large body at a very high temperature (>6000 degree Celsius on the Surface). It

therefore radiates over a very broad frequency spectrum which includes frequencies we use for communications.

But, the sun is a variable star and undergoes cycles at peak of which electrical disturbances erupt. Though this noise comes from limited portions of the disk, it may still be order of magnitude greater than that received during periods of quiet sun.

**a.2.2. Cosmic noise** – Since distant stars are also have high temperatures, they radiate noise in the same manner as the sun. The noise thus received is called thermal noise and is distributed uniformly over the entire sky. We also receive noise from the center of our own galaxy and from other galaxies.

**a.3. Industrial noise** – Under this heading, sources such as automobile and aircraft ignition, electric motors and switching gears and other heavy machines are included. Fluorescent lights are powerful source of such noise and should not be used where sensitive reception or testing is being conducted. It obeys the general principle that the received noise increases as the receiver bandwidth is increased.

**b) Internal noise** – This is the noise created by any of the devices, active or passive, found in the receivers. It is randomly distributed over the entire radio spectrum, there is, on the average, as much of it at one frequency as at any other. The random noise power is proportional to the bandwidth over which it is measured.

**b.1. Thermal noise** – The noise generated in a resistance or the resistive component of any impedance is random and is referred to as thermal, white or Johnson noise [3, 4]. It is due to the rapid and random motion of molecules, atoms and electrons of which any resistor is made up. The average noise power generated by a resistor is proportional to its absolute temperature and the bandwidth over which the noise is to be measured.

It is given as

$$P_n = kTB \quad (1)$$

Where k = Boltzmann's constant

T = absolute temperature in °K

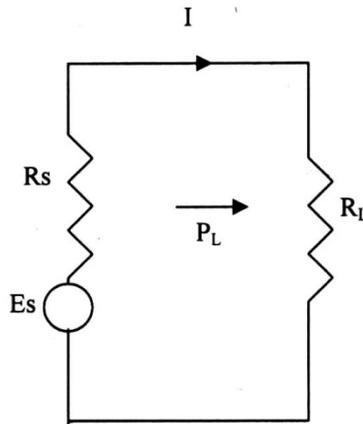
B = bandwidth of interest

$P_n$  = maximum noise power output of a resistor

The resistor is a noise generator and there may even be quite large voltage across it, however, since it is random and therefore has a definite r.m.s. value but no dc component, only the ac meter will register a reading.

Consider the voltage equivalent circuit as shown in Figure 1. The average power delivered by a voltage generator of internal r.m.s. voltage  $E_s$  and internal resistance  $R_s$  to a load R, when matched ( $R_s = R_L$ ) is maximum and given by

$$P_{L \max} = \frac{E_s^2}{4R_s} \quad (2)$$



**Fig. 1:** Voltage generator of internal r.m.s. voltage  $E_s$  and internal resistance  $R_s$  connected with a load resistance  $R_L$ .

## b.2. Channel Thermal noise in MOSFETs

MOSFETs are finding applications in integrated high frequency (HF) analog electronics and wireless communication. Since channel thermal noise is dominant at high frequencies, so accurate dc modeling is required to predict the HF noise performance of submicron MOSFETs. The present analytical model for a fully depleted MOSFET does not involve any empirical constants and is capable of predicting thermal noise behavior of long as well as short channel devices in both the linear and saturation regions [5,6]. The hot electron effect and the dependence of mobility on lattice temperature which arises due to the poor dissipation capability from the buried oxide structure have been incorporated in the analysis. The channel length modulation (CLM) has also been considered so as to accurately predict the high frequency noise performance of short channel devices. The results obtained are in good agreement with the experimental data [7].

## 2. THEORY

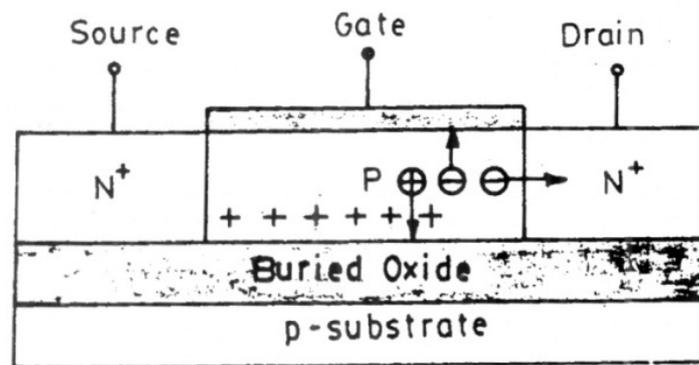
### 2.1. Hot Carrier Effects

When the channel length is reduced, while keeping the supply voltage constant, the maximum electric field experienced by the carriers in the channel region near the drain end is increased. As the carriers move from source to drain, they acquire enough kinetic energy in the high field region of the drain junction and cause impact ionization. Some of them can even surmount the Si-SiO<sub>2</sub> interface barrier and enter into the oxide. These high energy carriers that are no longer in thermal equilibrium with the lattice, and have energy higher than the thermal energy are called hot carriers. Effects arising from

heating of carriers in the channel under normal MOSFET operation are called channel hot-carrier effects [8,9].

When the impact ionization occurs, a primary hot carrier will generate a secondary electron-hole pair. While the electrons continue to constitute drain-to-source current, the secondary holes generated by the impact ionization drift through the body resulting in a so called the body current. A low level of body current will cause no undesirable effect. However, if the body current from a single MOSFET or the sum of the body currents from a large number of MOSFET's is excessively high, the body current as shown in Figure 2 will potentially saturate and raise the body potential and lead to circuit malfunctioning [10,11]. An excessive body current flowing through the body will result in an ohmic voltage drop in the body can forward bias the source to body junction. When coupled with the drain, a parasitic bipolar transistor exists in parallel with the MOSFET.

This composite drain to source breakdown in short channel MOSFETs results in snap back characteristic of the current-voltage curves. In CMOS circuits, the same mechanism can trigger a similar phenomena in a latchup.



**Fig. 2:** Schematic representation of hot carrier effects in a region of high longitudinal electric field in the channel of an n-type MOSFET.

## 2.2. Thermal noise in a conducting channel

The general expression of drain current of an MOSFET operating in strong inversion is

$$I_D = wQ_I(x)v(x) \quad (1)$$

where  $x$  is the position along the channel,  $w$  is the effective channel width,  $Q_I(x)$  is the inversion layer charge per unit area and  $v(x)$  is the carrier drift velocity in channel and can be written as

$$v(x) = \frac{\mu_{effo}E(x)}{1 + \frac{E(x)}{E_c}} \quad \text{when } E(x) < E_c \quad (2)$$

where  $\mu_{effo}$  is the effective surface mobility,  $E(x) = dV(x)/dx$  is the lateral electric field,  $E_c$  is the critical field at which the carrier velocity saturates and  $v(x)$  is the voltage at any point along the channel. The critical field and the effective surface mobility are given by

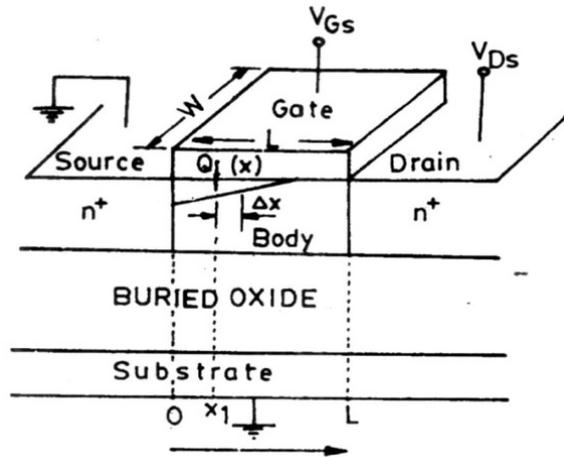
$$E_c = \frac{2v_{sat}}{\mu_{effo}} \quad (3)$$

And 
$$\mu_{effo} = \frac{\mu_o}{1 + \theta(V_{gs} - V_{th})} \quad (4)$$

where  $\mu_o$  is the low-field mobility,  $\theta$  is the mobility degradation coefficient due to the vertical channel field,  $V_{th}$  is the threshold voltage at the source end of the channel with zero source substrate bias and  $V_{gs}$  is the gate to source voltage drop of an intrinsic device.

The saturation velocity,  $v_{sat}$  of the carriers in the channel is approximately  $10^7$  cm/s at 300 K. Substituting (2) in (1) for  $E(x) < E_c$  and rearranging the equation, we get drain current  $I_D$  as

$$I_D = \left( \mu_{effo} W Q_l(x) - \frac{I_D}{E_c} \right) \frac{dV(x)}{dx} \quad (5)$$



**Fig. 3:** Schematic diagram of an n-type MOSFET.

On integrating (5) over the channel length, 0 to L, provide  $I_D$  is independent of position  $x$  and solving for  $I_D$  we get

$$\int_0^L I_D dx = \int_0^{V_{th}} \left( \mu_{effo} w Q_I(V) - \frac{I_D}{E_c} \right) dV(x) \quad (6)$$

or

$$I_D = \frac{1}{L} \int_0^{V_{ds}} \left( \mu_{effo} w Q_I(V) - \frac{I_D}{E_c} \right) dV(x) \quad (7)$$

The value of  $Q_I(V)$  depends upon the model used.

From (7) we see that if there is a time varying voltage fluctuation  $\Delta v(t)$  caused by the thermal noise in a unit length segment of the channel, then the current fluctuation  $\Delta i(t)$  caused by  $\Delta v(t)$  is given by

$$\Delta i(t) = \frac{1}{L} \left( \mu_{effo} w Q_I(V) - \frac{I_D}{E_c} \right) \Delta v(t) \quad (8)$$

as long as the variation of  $\Delta v(t)$  is slow enough so that quasi-static behavior is maintained. If  $\Delta v(t)$  is negligibly small,  $Q_I(V)$  is more or less a constant and independent of  $\Delta v(t)$ . The mean square value of  $\Delta i(t)$  will be given by

$$\overline{(\Delta i)^2} = \frac{1}{L^2} \left( \mu_{effo} w Q_I(V) - \frac{I_D}{E_c} \right)^2 \overline{(\Delta v)^2} \quad (9)$$

From (5) it can be shown that resistance  $\Delta R$  of a small element of length  $\Delta x$  centered around  $x = x_1$ (Fig.4.05) is

$$\Delta R = \frac{\Delta x}{\left( \mu_{effo} w Q_I(V) - \frac{I_D}{E_c} \right)} \quad (10)$$

where  $\Delta V = I_D \Delta R$  and  $x_1$  is the position along the length of the channel. Assuming that a small element of the channel acts a resistor of resistance  $\Delta R$ , we can find a small voltage  $\Delta v(t)$  across it. Now, the power spectral density of the noise voltage generated across a resistor of value  $R$  is  $4kTR$  for frequencies at which  $hf/kT \ll 1$ , where  $h$  is the Planck's constant and  $f$  is the frequency of the signal. Therefore the mean square value of  $\Delta v(t)$  is given as

$$\overline{(\Delta v)^2} = \frac{4kT_e(x_1) \Delta f \Delta x}{\left( \mu_{effo} w Q_I(x_1) - \frac{I_D}{E_c} \right)} \quad (11)$$

where  $T_e(x_1)$  is the effective electron temperature at  $x_1$ . Now, for long channel devices, the channel does not show any hot electron effects,  $T_e$  would be the same as the lattice temperature. Substituting (11) in (9) we get

$$\overline{(\Delta i)^2} = \frac{4kT_e(x_1)}{L^2} \left( \mu_{effo} w Q_I(V) - \frac{I_D}{E_c} \right) \Delta f \Delta x \quad (12)$$

This gives the contribution of the small element at  $x_1$  to the drain current noise. Letting  $\Delta x$  become a differential, integrating over the effective channel length and changing the variable  $dx$  to  $dV$  according to (5), the power spectral density of thermal noise in a channel,  $S_{ID}$  is given as

$$S_{ID} = \frac{4k}{L^2 I_D} \int T_e(x) \left( \mu_{effo} w Q_I(V) - \frac{I_D}{E_c} \right)^2 dV \quad (13)$$

Equation (13) includes velocity saturation effects and hot electron effects and is a general expression of thermal noise in the channel.

The electron temperature does not remain constant but increases with the electric field strength and can be written as

$$\frac{T_e(x)}{T_a} = \left( 1 + \frac{E(x)}{E_c} \right)^n \quad (14)$$

where  $0 \leq n \leq 1$ ,  $E(x)$  is the lateral electric field and  $T_a$  is the ambient temperature. Solving for  $E/E_c$  from (1), (2) and (5) and using  $E(x) = dV(x)/dx$ , we get

$$1 + \frac{E(x)}{E_c} = \frac{\mu_{effo} w Q_I(V)}{\mu_{effo} w Q_I(V) - \frac{I_D}{E_c}} \quad (15)$$

Now, using (15) in (13), we get

$$S_{ID} = \frac{\overline{i_d^2}}{\Delta f} = \frac{4kT_a}{L^2 I_D} \int_0^{V_{th}} (\mu_{effo} w Q_I(V))^n \left( \mu_{effo} w Q_I(V) - \frac{I_D}{E_c} \right)^{2-n} dv \quad (16)$$

In (14),  $n = 0$  corresponds to the absence of charge carrier heating while  $n = 1$  or  $2$  implies that the carrier heating is switched on which is the case with fully depleted MOSFET. Incorporating the temperature dependence, the spectral density of channel thermal noise is expressed in (16) where  $\overline{i_d^2}$  is the mean square value of drain current and  $\Delta f$  is the bandwidth. The above expression does not incorporate the lattice temperature dependence of mobility and the channel length modulation which play an important role in submicron fully depleted MOSFETs. Due to the buried oxide structure, self heating of a fully depleted MOSFET should not be overlooked. Due to heating effect, the temperature of the silicon film rise above the ambient temperature [12,13].

On solving (16), the power spectral density of channel thermal noise for different values of  $n$  in the linear region is given by

For  $n = 2$ ,

$$S_{ID2} = \frac{4kT_a \mu_{eff}^2 w^2 C ox^2}{L^2 I_D} \left[ (V_{gs} - V_{th})^2 V_{ds} + \frac{V_{ds}^3}{3} - (V_{gs} - V_{th}) V_{ds}^2 \right] \quad (17a)$$

For  $n = 1$ ,

$$S_{ID1} = S_{ID2} + \frac{4kT_a C_{ox} \mu_{eff} w}{L^2 E_c} \left[ (V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (17b)$$

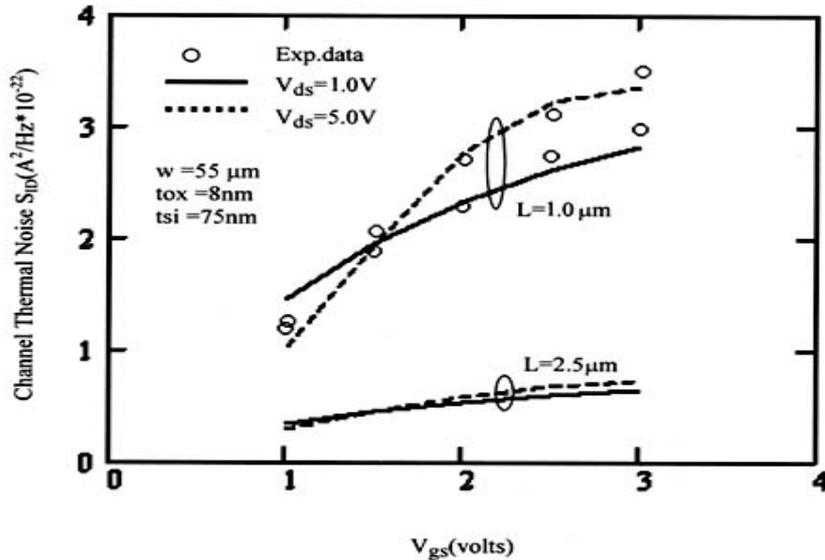
For  $n = 0$ ,

$$S_{ID0} = S_{ID2} + \frac{4kT_a I_D V_{ds}}{L^2 E_c^2} + \frac{8kT_a C_{ox} \mu_{eff} w}{L^2 E_c} \left[ (V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (17c)$$

Equation (17) is valid for the bias conditions at which the lateral electric field at any position in the conducting channel is smaller than  $E_c$  (i.e. the channel pinches off before carriers reach velocity saturation). The power spectral density of channel thermal noise for the saturation region can be obtained by replacing  $V_{ds}$  with  $V_{dsat}$  and  $L$  with  $L_{eff}$  in (17). Here, the value  $n = 2$  is taken to calculate spectral density of channel thermal noise because it gives results close to the experimental data [14,15].

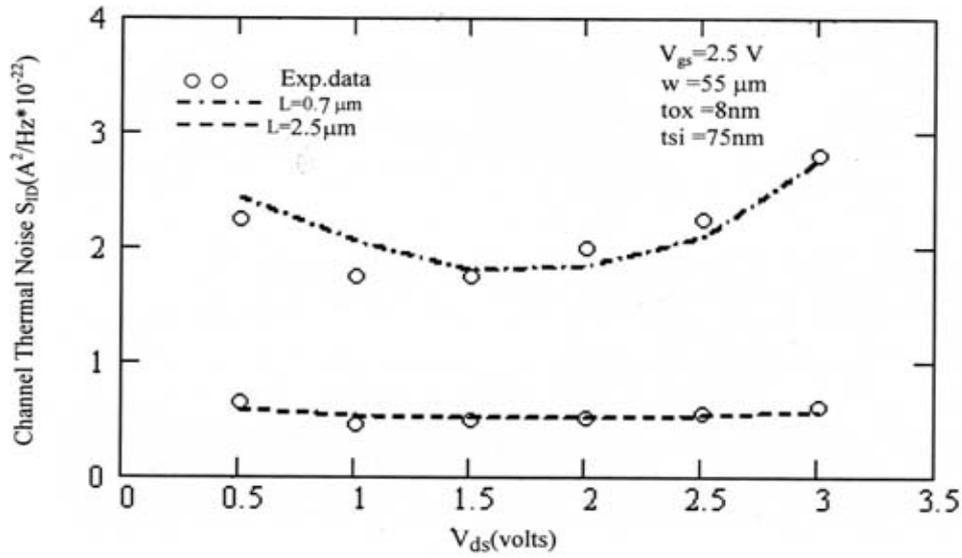
### 3. RESULTS AND DISCUSSION

Figure 4 shows the variation of channel thermal noise with gate to source voltage at  $V_{ds} = 1\text{ V}$  and  $5.0\text{ V}$ , for gate lengths  $L = 0.7\text{ }\mu\text{m}$  and  $L = 2.5\text{ }\mu\text{m}$  and the results so obtained match well with the experimental data. In long channel device, the inversion layer charge increases with  $V_{gs}$  leading to an increase in conductance and the channel thermal noise,  $S_{ID}$  also increases with  $V_{gs}$ . In short channel devices, the effective channel length decreases due to channel length modulation (CLM) and the conductance increases. The correct value of conductance in short channel thin film devices cannot be predicted at large gate voltage ( $V_{gs}$ ) because it leads to negative output conductance and can only be predicted if lattice temperature is considered. Therefore, considering CLM and lattice temperature effect, the channel thermal noise,  $S_{ID}$  increases as the effective conductance increases with  $V_{gs}$ .



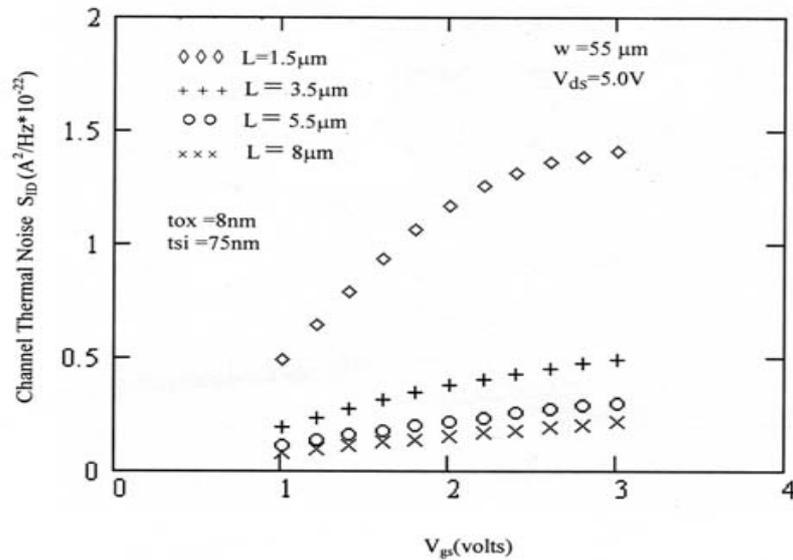
**Fig. 4:** Dependence of channel thermal noise ( $S_{ID}$ ) on gate bias for FD MOSFET,  $t_{ox}=8\text{ nm}$ ,  $t_{si}=75\text{ nm}$  and  $w=55\text{ }\mu\text{m}$ , for different gate lengths at  $V_{ds}=5.0\text{ V}$  and  $1.0\text{ V}$ .

Figure 5 shows the variation of channel thermal noise with drain to source voltage for gate lengths  $L = .70 \mu m$  and  $L=2.5\mu m$  and the results obtained are very close to the experimental data. For a long channel device, conductance is maximum in the triode region, i.e. at low  $V_{ds}$  and the noise is maximum. It then decreases with the increase in  $V_{ds}$  due to decrease in conductance, but it remains almost constant in the saturation region. In short channel devices (considering CLM and lattice temperature effect), the noise decreases with  $V_{ds}$  and reaches its minimum value and then increases with  $V_{ds}$ .



**Fig. 5:** dependence of channel thermal noise ( $S_{ID}$ ) on drain bias for FD MOSFET,  $t_{ox}=8nm$ ,  $t_{is}=75nm$  and  $w=55\mu m$ , for different gate lengths.

Figure 6 shows the variation of channel thermal noise with  $V_{gs}$  for different gate lengths at  $V_{ds} = 5.0V$ . It is clear from the figure that as the gate length reduces, the channel thermal noise,  $S_{ID}$  increases due to CLM effect.



**Fig. 6:** Dependence of channel thermal noise ( $S_{ID}$ ) on gate bias for FD MOSFET,  $t_{ox}=8\text{nm}$ ,  $t_{si}=75\text{nm}$  and  $w=55\mu\text{m}$ , for different gate lengths at  $V_{ds}=5.0\text{V}$ .

#### 4. CONCLUSION

This MOSFET model takes into account various short channel effects, such as, hot electron effect, lattice temperature dependent mobility and channel length modulation. The results so obtained have been compared with experimental data available in the literature and shows good agreement, thus proves the validity of the model.

#### REFERENCES

- [1] J.-P. Colinge; "Silicon-on-Insulator Technology: Materials to VLSI", 2<sup>nd</sup> Edition, Kluwer Academic Publishers, 2002.
- [2] J.B. Kuo and K.-W. Su; "CMOS VLSI Engineering: Silicon-on-Insulator (SOI)", Kluwer Academic Publishers, November 1998.
- [3] G. Knoblinger, P. Klein and M. Tiebout; "A new model of thermal channel noise of deep submicron MOSFTs and its application in RF-CMOS design", 2002. DOI: 10.1109/VLSIC.2000.852876.
- [4] S. Tedja, J.V. Spiegel and H.H. William; "Analytical and experimental studies of thermal noise in MOSFETs", IEEE Trans. On Electron Devices, Vol. 41(11), pp. 2069-2075, 1994.
- [5] P. Klein; "An analytical thermal noise model of deep submicron MOSFETs", IEEE Electron Device Letter, Vol. 20(8), pp. 399-401, 1999."

- [6] Y. Cheng, C.-H. Chen, M. Matloubian and M.J. Deen; "High frequency small signal AC and noise modeling of MOSFETs for RF IC design", IEEE Trans. On Electron Devices, Vol. 49(3), pp. 400-408, 2002.
- [8] B. Wang, J.R. Hellums and C.G. Sodini; "MOSFET thermal noise modeling for analog integrated circuits", IEEE Journal of Solid State Circuits, Vol. 29(7), pp. 833-835, 1994.
- [9] C.H. Chen and M.J. Deen; "High frequency noise of MOSFETs I Modeling", Solid State Electronics, Vol. 42(11), pp. 2069-2081, 1998.
- [10] N. Kapoor, S. Haldar, M. Gupta and R.S. Gupta; "Self-Heating-Dependent Thermal-noise model using distributed gate structure for RF applications", Microwave and Optical Technology Letters, Vol. 40(1), pp. 87-92, 2004.
- [11] Y.-G. Chen, S.-Y. Ma, J.B. Kuo, Z. Yu and R.W. Dutton; "An analytical drain current model considering both electron and lattice temperatures simultaneously for deep submicron ultrathin SOI NMOS devices with self heating", IEEE Trans. On Electron Devices, Vol. 42(5), pp. 899-906, 1995.
- [12] Jacob Millman, Christos C. Halkias; "Intergrated Electronics: Analog and Digital Circuits and Systems", McGraw-Hill electrical and electronic engineering series, 1972.
- [13] R.L. Boylested and L. Nashelsky; "Electronic devices and circuit theory".
- [14] B.G. Streetman; "Solid State Electronic devices".
- [15] S.M. Jze; "VLSI Technology".